IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2024

CIRCUITS AND SYSTEMS

Tuesday 14 May 14:30

Time allowed: 2 hours

There are THREE questions on the paper.

Answer ALL questions.

Any special instructions for invigilators and information for Candidates are on page 1.

Examiners responsible First Marker(s): P.Y.K. Cheung

Second Marker(s): A. Zhao

Information for Candidates:

The following notation is used in this paper:

1. Unless explicitly indicated otherwise, digital circuits are drawn with their inputs on the left and their outputs on the right.
2. Within a circuit, signals with the same name are connected together even if no connection is shown explicitly.
3. The notation X[2:0] denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0.

1. (a) Consider the circuit shown in *Figure 1.1(a).*

(i) Derive the equation that relates the output signal $y(t)$ to the input signal $x(t)$.

[4]

(ii) Given that R = 1kΩ and C = 10nF, and that the input $x(t)$ is a square wave as shown in *Figure 1.1(b),* sketch the output signal $y(t)$.

[6]

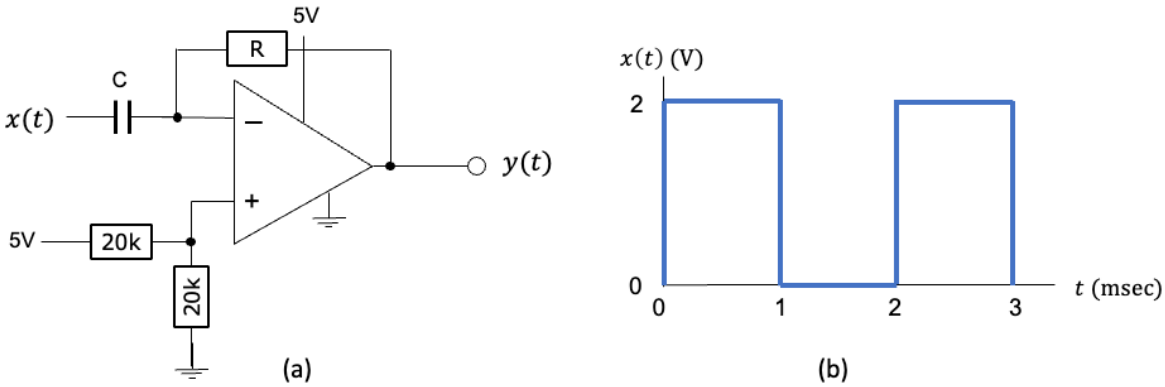

Figure 1.1

(b) *Figure 1.2* shows the SystemVerilog specification of a finite state machine FSM with four states that uses one-hot encoding.

(i) What is one-hot encoding? Briefly explain why one-hot encoding is particularly suitable for FPGA implementations.

[3]

(ii) Construct the state diagram for this FSM.

[3]

(iii) Complete the timing diagram for the FSM as shown in *Figure 1.3* to include the state and the output signal *Y*.

[4]

```
module FSM (
    input  logic    clk,    // clock
    input  logic    rst,    // reset state machine
    input  logic    A,      // input signal
    output logic    Y       // output signal
);

    // define states
   parameter    NSTATE = 4;
   parameter    S0 = 4'b0001;
   parameter    S1 = 4'b0010;
   parameter    S2 = 4'b0100;
   parameter    S3 = 4'b1000;

    logic [NSTATE-1]    current_state, next_state;

    // state registers
    always_ff @(posedge clk)
        if (rst)    current_state <= S0;
        else        current_state <= next_state;

    // next state logic
    always_comb
        case (current_state)
            S0: next_state = S1;
            S1: if (A==1'b1) next_state = S2;
                else next_state = S3;
            S2: next_state = S3;
            S3: if (A==1'b1) next_state = S1;
                else next_state = S0;
        default: next_state = current_state;
        endcase

    // output logic
    always_comb
        case (current_state)
            S0: Y = 1'b0;
            S1: Y = !A;
            S2: Y = 1'b1;
            S3: Y = A;
        default: Y = 1'b0;
        endcase

endmodule
```

Figure 1.2

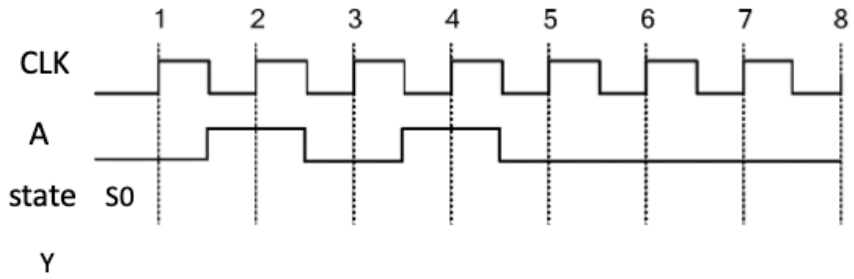

Figure 1.3

(c) A microprocessor system has an 16-bit memory address bus and an 8-bit data bus. The system consists of two banks of ROMs, ROM_1 and ROM_2, and one bank of RAM.

The two banks of ROMs are 8kB and 16kB in size and with addresses starting at 16'hE000 and 16'h8000 respectively. The RAM is 32kB in size and occupies the address space starting at 16'h0000. The input/output space (IO) occupies 32-byte addresses starting at 16'hDFE0.

(i) Draw the memory map for the microprocessor system showing the starting and ending addresses for ROM_1, ROM_2, RAM and IO.

[4]

(ii) *Figure 1.4* shows the interface specification for an address decoder module in SystemVerilog that decodes the address bus and produces enable signals for ROM_1, ROM_2, RAM and IO. Design the address decoder module in SystemVerilog.

[6]

```
module addr_decoder (
    input  logic    [15:0]  A,       // address input
    output logic            ROM_1,      // ROM 1 select
    output logic            ROM_2,      // ROM 2 select
    output logic            RAM,        // RAM select
    output logic            IO          // IO select
)
```

Figure 1.4

(d) For the FPGA circuit shown in *Figure 1.5*, the clock to output delay t_p of the flip-flops is 1 ns, and the setup and hold time are $t_s = 2$ ns and $t_h = 1$ ns respectively. The propagation delay of LUT *X* is in the range 2 ns < t_X < 3 ns. It is further known that the clock buffer circuit *Y* has a propagation delay in the range 1 ns < t_Y < 2 ns. The clock signal *CLK* is symmetrical with period T.

(i) Given that the timing waveforms for signals A and CLK are as shown in *Figure 1.6*, draw the timing waveforms for signals B, C, D and E showing all the delay values. You may assume that signals B, D and E are initially low.

[4]

(ii) Derive the inequalities for the setup times applied to flip-flop FF2.

[4]

(iii) Hence or otherwise, derive the maximum clock frequency for the circuit.

[2]

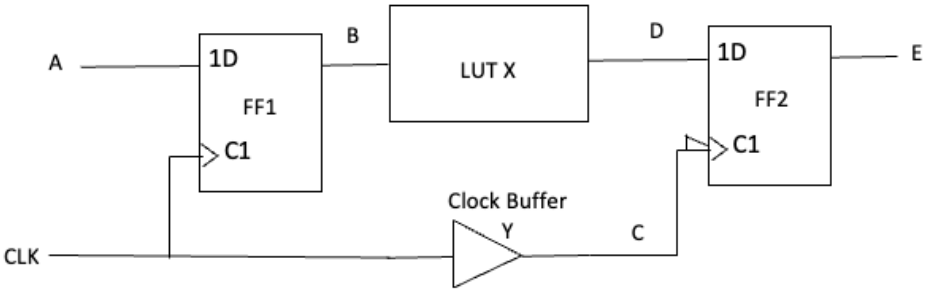

Figure 1.5

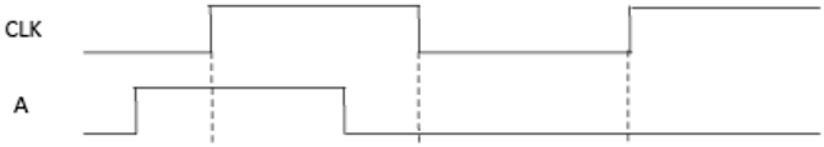

Figure 1.6

(e) (i) Explain the meaning of the following specifications for a digital-to-analogue converter (DAC): *resolution*, *monotonicity* and *settling time*.

[3]

(ii) You are required to convert a 10-bit digital number to an analogue voltage over the voltage range of 0 to 3.3V with a Digital-to-Analogue Converter (DAC). What is the resolution of the analogue output?

[2]

(iii) *Figure 1.7* shows the circuit of a 4-bit DAC using a R-2R ladder circuit, four electronic switches and a current summing operational amplifier.

Derive the value I_O flowing through the bottom resistor. What is the output voltage V_{out} of the DAC with the switch setting as shown in *Figure 1.7*?

[5]

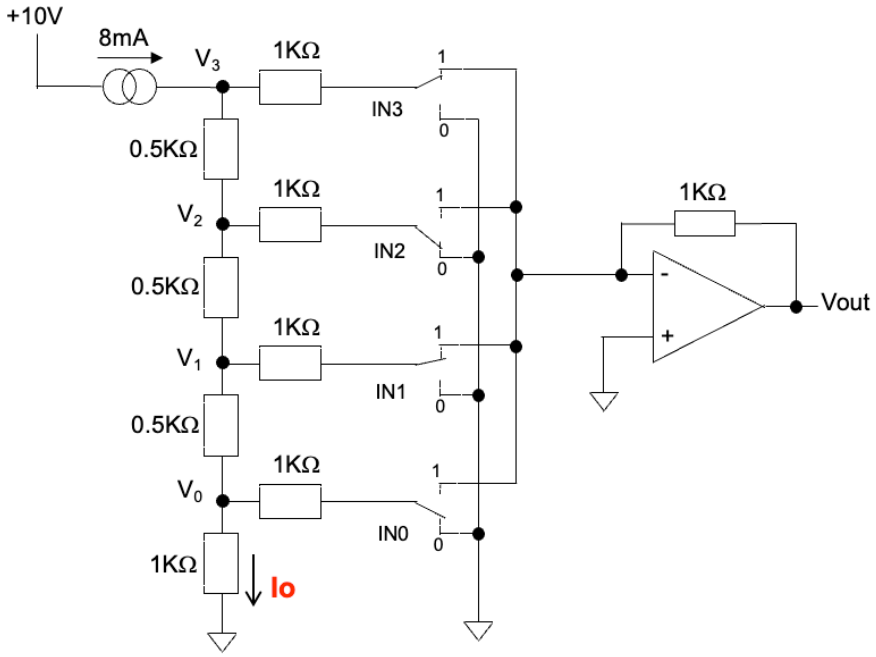

Figure 1.7

2. *Figure 2.1* shows a function generator circuit using three identical operational amplifiers IC1 to IC3 that are designed to use single power supply and are capable of rail-to-rail output voltage swing.

(a) What are the threshold voltages at V_1 that cause the output V_2 of IC2 to change state?

[6]

(b) The output voltage V_2 is a square signal between 0V and 5V the frequency of which can be changed between 166.7Hz and 200Hz by adjusting the variable resistor RV1. Derive the values of the resistor R1 and the variable resistor RV1.

[12]

(c) V_3 is a DC voltage at 3V and RV1 is set to be at the mid-position of the variable resistor. Sketch the waveforms for V_1 and V_4. Your answer must show the key voltages and time points for one cycle of the repetitive signals.

[7]

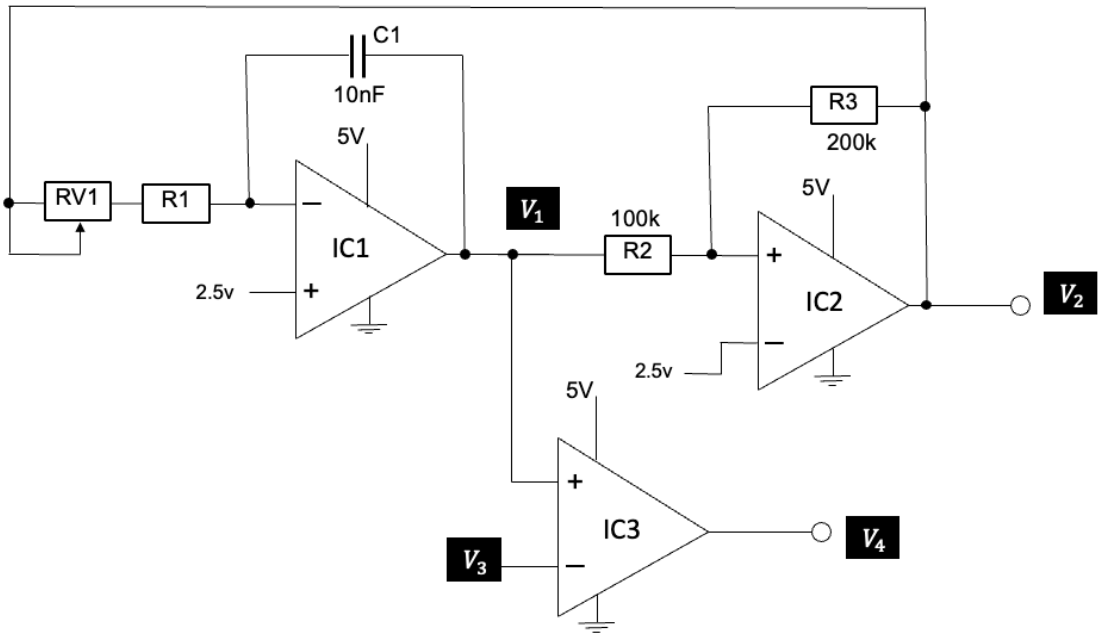

Figure 2.1

3. *Figure 3.1* shows a circular magnet with 8 pairs of N and S poles attached to the axle of a DC motor. Two Hall effect sensors A and B are arranged to sense the magnetic flux. As the North pole of the magnet passes a sensor, a pulse is produced. The two sensors are also mounted offset from each other such that the phase of the two signals is as shown in *Figure 3.2*. When the motor is rotating in the counter-clockwise direction, the sensor A signal leads the sensor B signal by 90° phase. The opposite is true when the motor is rotating in the clockwise direction. The outputs of the two sensors are used to form a 2-bit state value as shown in the diagram.

   (a) Design, in the form of a state diagram, a finite state machine (FSM) that detects the direction of the rotation of the motor.

   [10]

   (b) Implement your FSM in SystemVerilog.

   [15]

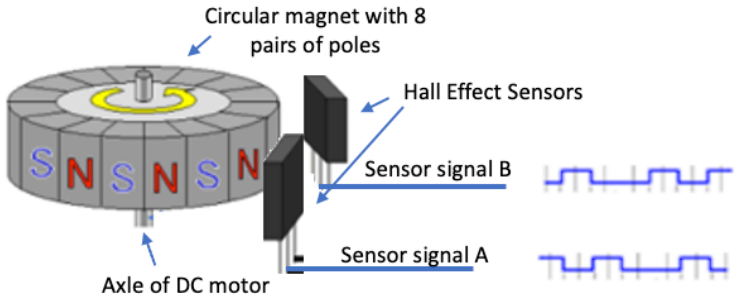

Figure 3.1

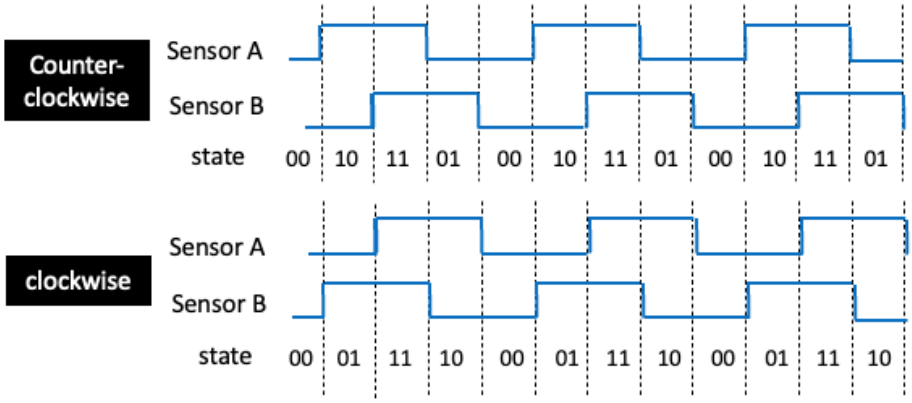

Figure 3.2

